Claim Amendments

Please amend claims 1-3, 6-10, 2, 12, 14, and 16-18 as follows.

Please cancel claims 15 and 20 as follows.

Please add new claims 21-26 as follows.

1. (currently amended) A method for forming a dual damascene structure in a semiconductor device manufacturing process comprising the steps of:

providing a process wafer comprising a via opening extending through at least one dielectric insulating layer;

~~blanket depositing~~ forming a first photoresist layer on the process wafer surface to include filling the via opening;

~~blanket depositing~~ forming a second photoresist layer ~~over and contacting~~ on the ~~negative~~ first photoresist layer;

photolithographically~~y~~ patterning the ~~positive~~ second photoresist layer to form a trench opening etching pattern; ~~overlying and encompassing the via opening and the first photoresist layer to form~~

forming a via plug comprising the first photoresist layer wherein the first and second photoresist layers respectively comprise different types of photoresist selected from the group consisting of positive and negative photoresists; and,

~~etching back the negative photoresist layer to form a via plug having a predetermined thickness partially filling the via opening; and,~~

etching a trench opening according to the trench opening etching pattern.

2.(currently amended) The method of claim 1, further comprising carrying out a plasma ashing process to remove remaining portions of the ~~negative~~ first photoresist layer and the ~~positive~~ second photoresist layer following the step of etching a trench opening.

3. (currently amended) The method of claim 1, wherein the steps of ~~etching back~~ forming a via plug and etching a trench opening are carried out in-situ according to a plasma assisted etching process.

4. (original) The method of claim 1, wherein the at least one dielectric insulating layer comprises a lower dielectric insulating layer and an upper dielectric insulating layer separated by a middle etch stop layer.

5. (original) The method of claim 1, wherein the via plug is formed to fill the via opening to a level at about where a bottom portion of the trench opening is formed.

6. (currently amended) The method of claim 1, wherein ~~an uppermost dielectric layer of~~ the at least one dielectric insulating layer is provided with an uppermost layer selected from the group consisting of ~~at least one of an overlying~~ a bottom anti-reflective coating (BARC) layer and an etch stop layer.

7. (currently amended) The method of claim 6, wherein the ~~BARC~~ uppermost layer comprises ~~at least~~ an inorganic layer selected from the group consisting of silicon oxynitride, silicon oxycarbide, and titanium nitride.

8. (currently amended) The method of claim 6, wherein the ~~BARC~~ uppermost layer is etched through to expose the at least one dielectric insulating layer during the step of ~~etching back~~ forming a via plug.

9. (currently amended) The method of claim 1, further comprising the step of curing the first photoresist layer according to a curing process selected from the group consisting of ~~at least one a~~ photo-curing and [[a]] thermal curing ~~process to harden the negative photoresist according to polymeric cross-linking reactions~~ following the step ~~of blanket depositing~~ forming a ~~negative~~ first photoresist layer.

10. (currently amended) The method of claim 9, wherein the ~~negative~~ first photoresist layer is cured in a nitrogen containing ambient.

11. (original) The method of claim 1, wherein the at least one dielectric insulating layer comprises a low-K dielectric insulating layer selected from the group consisting of fluorine doped silicon oxide, carbon doped silicon oxide, and organo-silane glass.

12. (currently amended) A method for forming a dual damascene structure in a semiconductor device manufacturing process comprising the steps of:

providing a process wafer comprising a via opening extending through at least one dielectric insulating layer and an uppermost bottom anti-reflective coating (BARC) layer;

~~blanket depositing~~ forming a ~~flowable~~ negative photoresist layer on the process wafer surface to include filling the via opening;

~~curing the flowable negative photoresist layer according to at least a photo-curing process;~~

~~blanket depositing~~ forming a positive photoresist layer ~~over and contacting~~ on the negative photoresist layer;

photolithographically patterning the positive photoresist layer to form a trench opening etching pattern overlying and encompassing the via opening;

~~plasma~~ etching ~~back~~ the negative photoresist layer to form a via plug having a predetermined thickness ~~partially filling~~ the ~~via opening~~;

~~plasma~~ etching in-situ ~~with respect to the step of etching back~~ a trench opening according to the trench opening etching pattern; and,

carrying out a plasma ashing process to remove remaining portions of the via plug and the positive photoresist layer.

13. (original) The method of claim 12, wherein the at least one dielectric insulating layer comprises a lower dielectric insulating layer and an upper dielectric insulating layer separated by a middle etch stop layer.

14. (currently amended) The method of claim 12, wherein the ~~via plug is formed to fill the via opening to~~ the predetermined thickness is at a level at about where a bottom portion of the trench opening is formed.

15. (cancelled)

16. (currently amended) The method of claim 12, wherein the BARC layer comprises ~~at least~~ an inorganic layer selected from the group consisting of silicon oxynitride, silicon oxycarbide, and titanium nitride.

17. (currently amended) The method of claim 12, wherein the BARC layer is etched through to expose the at least one dielectric insulating layer during the step of etching ~~back~~ the negative photoresist layer.

18. (currently amended) The method of claim 12, ~~wherein~~ further comprising the step of curing the negative photoresist following the step of forming a negative photoresist layer ~~the step of curing is carried out in a nitrogen containing ambient~~.

19. (original) The method of claim 12, wherein the at least one dielectric insulating layer comprises a low-K dielectric insulating layer selected from the group consisting of fluorine doped silicon oxide, carbon doped silicon oxide, and organo-silane glass.

20. (cancelled)

21. (new) The method of claim 1, further comprising the step of filling the via and trench openings with a conductive material.

22. (new) The method of claim 12, further comprising the step of filling the via and trench openings with a conductive material.

23. (new) The method of claim 1, wherein the first photoresist layer comprises a negative photoresist and the second photoresist layer comprises a positive photoresist.

24. (new) The method of claim 1, wherein the first photoresist layer comprises a positive photoresist and the second photoresist layer comprises a negative photoresist.

25. (new) The method of claim 1, wherein the step of forming a via plug comprises etching back the first photoresist layer.

26. (new) The method of claim 1, wherein the via plug is formed to at least partially fill the via opening.